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-	57	(((((fault adj (test\$3 or simulat\$4)) and (test near4 (vector\$1 or pattern\$1 or sequence\$1 or list\$1)) and (((power adj suppl\$3) near4 current\$1) near\$3	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/10/28 17:59
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-	7	(((((fault adj (test\$3 or simulat\$4)) and (test near4 (vector\$1 or pattern\$1 or sequence\$1 or list\$1)) and (((power adj suppl\$3) near4 current\$1) near\$3	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/10/28 17:59
-	36	((fault adj (test\$3 or simulat\$4)) and (test near4 (vector\$1 or pattern\$1 or sequence\$1 or list\$1)) and (((power adj suppl\$3) same current\$1) same (transient\$2 or spike\$1 or surge\$1))	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/10/28 17:59
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1 A novel wavelet transform based transient current analysis for fault detection and localization

Bhunja, S.; Roy, K.; Segura, J.;

Design Automation Conference, 2002. Proceedings. 39th , 10-14

June 2002

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Wanli Jiang , Bapiraju Vinnakota

Proceedings of the 36th ACM/IEEE conference on Design automation conference June 19992 [Contest: a concurrent test generator for sequential circuits](#)

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Vishwani D. Agrawal , Kwang-Ting Cheng , Prathima Agrawal

Proceedings of the 25th ACM/IEEE conference on Design automation June 1988

This paper describes the application of a concurrent fault simulator to automatic test vector generation. As faults are simulated in the fault simulator a cost function is simultaneously computed. A simple cost function is the distance (in terms of the number of gates and flip-flops) of a fault effect from a primary output. The input vector is then modified to reduce the cost function until a test is found. The paper presents experimental results showing the effectiveness of this method in ...

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 Dirk Niggemeyer, Elizabeth M. Rudnick


ACM Transactions on Design Automation of Electronic Systems (TODAES) October 2003

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Systems-on-Chips often contain a large amount of embedded memory. In order to obtain sufficiently high yield, efficient diagnosis and repair facilities are needed for the memories. A novel and efficient approach for collecting complete failure data during on-chip memory testing is proposed that can be combined with a row/column reconfiguration algorithm for complete on-chip memory repair. A sequence of diagnostic tests of linear order is utilized that detects and localizes all cells involved in ...

2 [A circuit level fault model for resistive bridges](#)

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 Zhuo Li, Xiang Lu, Wangqi Qiu, Weiping Shi, D. M. H. Walker

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Delay faults are an increasingly important test challenge. Modeling bridge faults as delay faults helps delay tests to detect more bridge faults. Traditional bridge fault models are incomplete because these models only model the logic faults or these models are not efficient to use in delay tests for large circuits. In this article, we propose a physically realistic yet economical resistive bridge fault model to model delay faults as well as logic faults. An accurate yet simple delay calculation ...

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An approach to verify the knowledge base of a diagnostic expert system is described. An heuristic knowledge base collected from domain experts by interviews was analysed and the reasons for changes between versions were noted. The knowledge base was then compared with a small causal qualitative model of the device covered by the heuristic knowledge. Conclusions are drawn regarding the quality of the heuristic knowledge and indicate how it is planned to use the comparison of heuristic and ca ...

2 [Knowledge based fault management for OSI networks](#) 100% Celia A. Joseph , A. Sherzer , K. Muralidhar**Proceedings of the third international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 1** June 1990

The OSI Fault Management system (OSIFaM) is an evolving knowledge-based system for fault management of Open System Interconnection (OSI) networks. Our goal is to develop a knowledge-based tool that will reduce the expertise needed to recognize, diagnose and correct faults in OSI networks. For our first implementation, we are focusing on MAP 3.0 networks. This paper provides an overview of fault management in general, a brief survey of other fault management developments, the characteristics ...

3 [A data acquisition methodology for on-chip repair of embedded memories](#) 100% Dirk Niggemeyer , Elizabeth M. Rudnick

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1 An approach to dynamic power consumption current testing of CMOS ICs

Segura, J.A.; Roca, M.; Mateo, D.; Rubio, A.;

VLSI Test Symposium, 1995. Proceedings., 13th IEEE , 30 April-3 May 1995

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2 GOS defects in SRAM: fault modeling and testing possibilities

Segura, J.A.; Rubio, A.;

Memory Technology, Design and Testing, 1994., Records of the IEEE International Workshop on , 8-9 Aug. 1994

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3 CURRENT VS. LOGIC TESTING OF GATE OXIDE SHORT, FLOATING GATE AND BRIDGING FAILURES IN CMOS

Rodriguez-Montanes, R.; Segura, J.A.; Champac, V.H.; Figueras, J.; Rubio, J.A.;

Test Conference, 1991, Proceedings., International , 26-30 Oct 1991

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1 New atpg algorithm for iddt-based testing

Chehab, A.; Makki, R.; Maddali, R.;

Microelectronics, The 14th International Conference on 2002 - ICM ,
Dec. 11-13, 2002

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2 I_{DDT} testing of embedded CMOS SRAMs

Kumar, S.A.; Makki, R.Z.; Binkley, D.M.;

Design, Automation and Test in Europe Conference and Exhibition,
2002. Proceedings , 4-8 March 2002

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3 i_{DDT} test methodologies for very deep sub-micron CMOS circuits

Chehab, A.; Makki, R.; Spica, M.; Wu, D.;

Electronic Design, Test and Applications, 2002. Proceedings. The
First IEEE International Workshop on , 29-31 Jan. 2002

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4 SRAM test using on-chip dynamic power supply current sensor

Jian Liu; Makki, R.Z.;

Memory Technology, Design and Testing, 1998. Proceedings.
International Workshop on , 24-25 Aug. 1998

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5 Testing Embedded Memories: Is Bist The Ultimate Solution? Testing Of Embedded Memories-the Aggregate

Makki, R.Z.;

Test Symposium, 1998. ATS '98. Proceedings. Seventh Asian , 2-4 Dec. 1998
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6 Dynamic power supply current testing of CMOS SRAMs

Jian Liu; Makki, R.Z.; Kayssi, A.;

Test Symposium, 1998. ATS '98. Proceedings. Seventh Asian , 2-4 Dec. 1998
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7 A high level language implementation of a general purpose telemetry system for biomedical applications

Rorie, J.F.; Simmerman, J.K.; Makki, R.Z.; Piendl, R.D.;

System Theory, 1996., Proceedings of the Twenty-Eighth Southeastern Symposium on , 31 March-2 April 1996
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8 Transient power supply current testing of digital CMOS circuits

Makki, R.Z.; Shyang-Tai Su; Nagle, T.;

Test Conference, 1995. Proceedings., International , 21-25 Oct. 1995

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[\[Abstract\]](#) [\[PDF Full-Text \(864 KB\)\]](#) **IEEE CNF**

9 Power supply current detectability of SRAM defects

Jian Liu; Makki, R.;

Test Symposium, 1995., Proceedings of the Fourth Asian , 23-24 Nov. 1995
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10 Dynamic power supply current monitoring of SRAMs

Shyang-Tai Su; Makki, R.Z.; Nagle, H.T.; Jian Liu;

ASIC Conference and Exhibit, 1994. Proceedings., Seventh Annual IEEE International , 19-23 Sept. 1994
Page(s): 370 -373

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11 A testable static RAM structure for efficient coverage

pattern sensitive faults*Shyang-Tai Su; Makki, R.Z.;*

VLSI Test Symposium, 1992. '10th Anniversary. Design, Test and Application: ASICs and Systems-on-a-Chip', Digest of Papers., 1992
IEEE , 7-9 April 1992

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12 ON THE INTEGRATION OF DESIGN AND MANUFACTURING FOR IMPROVED TESTABILITY*Makki, R.Z.; Daneshvar, K.; Tranjan, F.; Greene, R.;*

Test Conference, 1991, Proceedings., International , 26-30 Oct 1991

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[\[Abstract\]](#) [\[PDF Full-Text \(488 KB\)\]](#) **IEEE CNF**

13 On controllability estimation to aid in partitioning logic circuits*Sern, J.; Makki, R.;*

Southeastcon '91., IEEE Proceedings of , 7-10 April 1991

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14 NEPTUNE: an automatic test pattern generator for finite state machines*Divekar, S.; Makki, R.Z.; Mostafavi, T.M.;*

Southeastcon '91., IEEE Proceedings of , 7-10 April 1991

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15 A VLSI based logic analyzer interface for a microprocessor development system*Lee, B.H.; Makki, R.Z.; Rohe, C.;*

System Theory, 1991. Proceedings., Twenty-Third Southeastern Symposium on , 10-12 March 1991

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Ramamurthy, H.; Karandikar, A.; Verma, R.;
Communication Systems, 2002. ICCS 2002. The 8th International
Conference on , Volume: 2 , 25-28 Nov. 2002
Page(s): 938 -942 vol.2

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2 I_{DD} pulse response testing on analog and digital CMOS circuits

Beasley, J.S.; Ramamurthy, H.; Ramirez-Angulo, J.; DeYong, M.;
Test Conference, 1993. Proceedings., International , 17-21 Oct. 1993

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3 i_{DD} pulse response testing: a unified approach to testing digital and analogue ICs

Beasley, J.; Ramamurthy, H.; Ramirez-Angulo, J.; Deyong, M.;
Electronics Letters , Volume: 29 Issue: 24 , 25 Nov. 1993
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Testing Mixed Signal Circuits and Systems (Ref. No: 1997/361), IEE Colloquium on , 23 Oct. 1997

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Power Electronics and Applications, 1993., Fifth European Conference on , 13-16 Sep 1993

Page(s): 191 -196 vol.8

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Power Electronics Specialist, 2003. PESC '03. IEEE 34th Annual Conference on , Volume: 2 , 15-19 June 2003

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[\[Abstract\]](#) [\[PDF Full-Text \(471 KB\)\]](#) **IEEE CNF**

4 CMOS IC stuck- pen-fault electrical effects and design considerations

Soden, J.M.; Treece, R.K.; Taylor, M.R.; Hawkins, C.F.;
Test Conference, 1989. Proceedings. 'Meeting the Tests of Time',
International , 29-31 Aug. 1989
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[\[Abstract\]](#) [\[PDF Full-Text \(624 KB\)\]](#) **IEEE CNF**

5 Performance analysis and signal processing in a current sensing power MOSFET (SENSEFET)

Yuvarajan, S.; Wang, L.;
Industry Applications Society Annual Meeting, 1991., Conference
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6 A novel high efficiency UPS using improved inverter and DC to DC converter

Eishima, Y.; Jinno, M.; Tominaga, F.; Sakamoto, H.; Harada, K.;
Telecommunications Energy Conference, 1991. INTELEC '91., 13th
International , 5-8 Nov. 1991
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7 Design and testing of power supplies for the high power gyrotron

Tsuneoka, M.; Fujita, H.; Nagashima, T.; Cho, Y.; Yamane, T.;
Hayakawa, S.; Ohtsuka, S.; Harada, K.; Yoshida, T.; Shibuya, T.;
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Fusion Engineering, 1991. Proceedings., 14th IEEE/NPSS Symposium
on , 30 Sept.-3 Oct. 1991
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8 Groundbounce in ASIC's: model and test results

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